EE335 Electronics

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**Q3.** (25) For the DC analysis of the JFET amplifier seen in Fig.3.a,

a) (04) determine the voltage VG.

b) (06) draw ID-VGS characteristics of the JFET transistor on a milimetric paper given in fig. 3.b.

c) (10) mark the operating point Q(IDQ, VGSQ) on the characteristics you have drawn in part c.

d) (05) find VD, VS and VDSQ.

**Q4.** (22) Consider again the same JFET amplifier of Fig. 3.a. For the AC analysis, determine the followings:

a) (04) Draw the AC equiv. circuit

**b)** (06) Calculate

**c)** (08) Derive the expression and calculate its value.

**d)** (04) Write down expression if .

Fig. 3.b

**0**

**VGS (V)**

|  |  |  |
| --- | --- | --- |
| Ii  **IDSS=6 mA**  **Vp=-3 V**  R1=108 MΩ  I0  Fig. 3.a.   |  | | --- | | **1**  **-3**  **-2**  **4**  **3**  **2**  **-1**  **100**  **8**  **6**  **4**  **2**  **ID (mA)** | | |
|
|  |

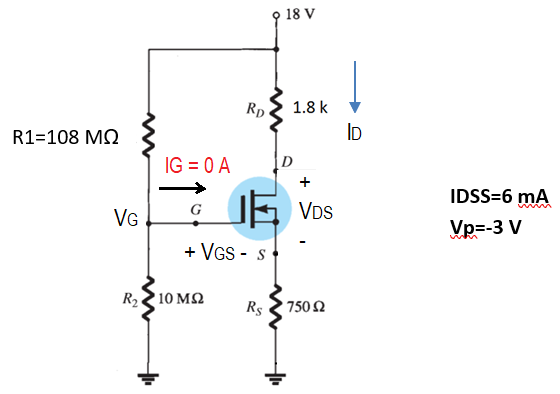
**SOLUTIONS**

**Q3.**

**a)** **DC ANALYSIS:** For this we do the followings:

- all caps. are to be “open-circuited”.

So, the “**DC eqvn. circuit”** would be as follows:



From the above circuit, we write

**b)** Drawing ID-VGS characteristics of the JFET transistor:

We must use the **Shockley’s equation** given by

Where IDSS and Vp are “drain saturation current” and “pinch-off voltage” of the JFET given in fig. 3.a as IDSS=6mA and Vp=-3V, respectively.

We need to calculate 4 critical points to be able to draw the JFET characteristics as in the following table:

|  |  |  |  |
| --- | --- | --- | --- |
| **Point** | **VGS** | **ID** | Coordinate at  (VGS,ID) |
| p1 | for **VGS=0** |  | **p1 = (0, 6 mA)** |
| p2 | for **VGS=**0.3Vp  = - 0.9 V |  | **p2 = ( - 0.9 V, 3 mA)** |
| p3 | for **VGS** =Vp/2  = - 1.5 V |  | **p3 = ( - 1.5 V, 1.5 mA)** |
| p4 | for **VGS=**Vp  = - 3 V |  | **p4 = ( - 3 V, 0 mA)** |

These 4 points are marked in the milimetric paper given in fig.3.b, and they are then combined to form the JFET characteristic. Fig. 3.b has been redrawn in the following fig.3.c with JFET characteristics on it.

**VGS (V)**

|  |
| --- |
| **3**  p3  1.5  p4  3  p2  **1**  **-3**  **-2**  **4**  **2**  **-1**  **100**  **8**  **6**  **4**  **2**  **ID (mA)** |

**VGS (V)**

-1.5 V

-0.9 V

Fig. 3.c. JFET characteristic.

**c)** mark the operating point Q(IDQ, VGSQ) on the characteristics you have drawn in part c.

**DETERMINING THE DC OPERATING POINT Q (VGSQ, IDQ):**

From the “**DC eqvn. circuit” we obtained in part a,** we write a KVL for the input as follows,

(1)

This is a line equation. We should draw this line on the JFET characteristics we have already plotted in fig. 3.c. Here is, how the procedure:

|  |  |  |  |
| --- | --- | --- | --- |
| point | Condition | Equation | Coordinate at (VGS, ID) |
| A | For ID=0 | VG=VGS, so VGS=VG=1.5254 V | (1.5254 V, 0 mA) |
| B | For VGS=0 V | VG=VGS + ID\*RS, So VG=ID\*RS.  Thus, ID=VG/RS=1.5254/(0.75 k)=2.034 mA | (0 V, 2.034 mA) |

You can now see the final status of the plot in fig. 3.d.

|  |
| --- |
| **Q**(VGSQ, IDQ)=  **Q**(-0.80 V, 3.2 mA)  1.5  B  p3  p4  3  p2  **1**  **-3**  **-2**  **4**  **3**  **2**  **-1**  **100**  **8**  **6**  **4**  **2**  **ID (mA)** |

A

**VGS (V)**

-1.5 V

-0.9 V

Fig. 3.d. JFET characteristic.

d) find VD, VS and VDSQ.

From the “**DC eqvn. circuit” we obtained in part a,** we write a KVL for the output as follows,

(2)

From which we obtain VDS as

From the fig.3.d, we read the Q-point as Q(VGSQ, IDQ)=**Q**(-0.80 V, 3.2 mA). Thus, VGSQ=-0.80 V, IDQ=3.2 mA. Therefore from (3), for VDD=18 V, IDQ=3.2 mA, RD=1.8 k, RS=0.75 k,

Since VDS=VD-VS, so we have

VD=VDS+VS

=9.84 + 2.4

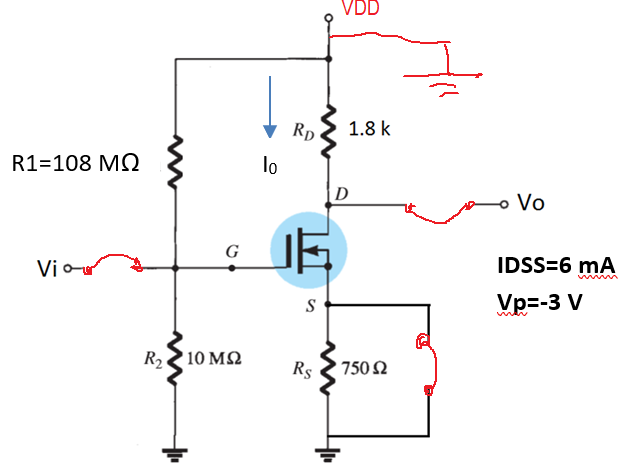
VD= 12.24 V

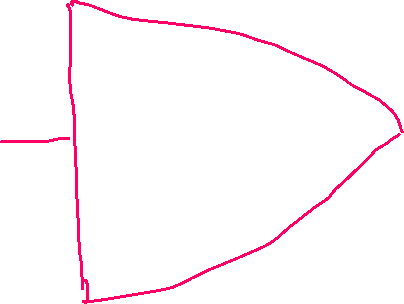
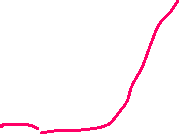
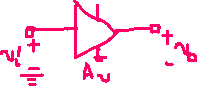
**Q4.**

1. **AC ANALYSIS:** The AC equivalent circuit is to be drawn. For this, we need to make the followings:

* All caps. are to be “short-circuited”.
* Supply source is to be grounded.

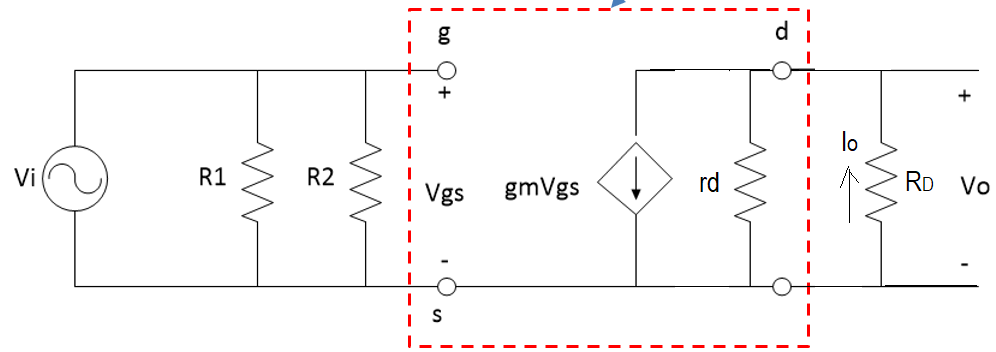
The resulting circuit would be as follows:





Ii

If the JFET transistor in the above circuit is replaced by its **AC eqvn. circuit** and the circuit is rearranged, the **“complete AC eqvn. circuit of the JFET amplifier”** would be as follows:





Ii

**Finding input impedance (Zi)**: from the AC eqvn. circuit we write;

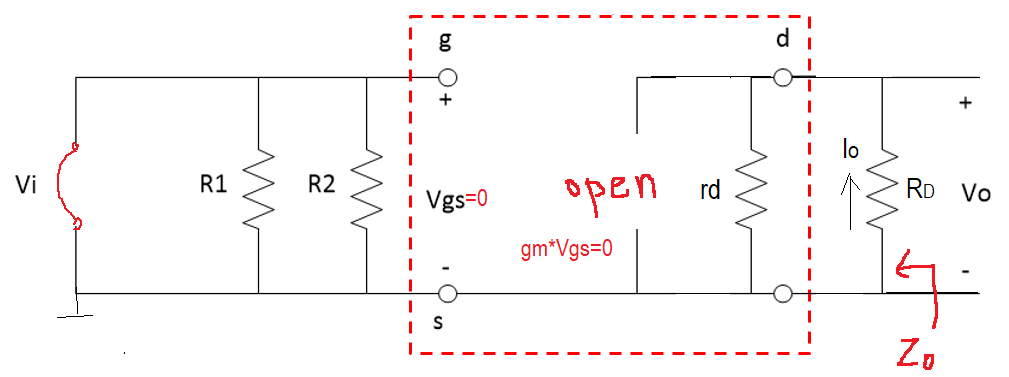


Zi= Vi/Ii=R1||R2 = 108 MΩ || 10 MΩ = 9.1525 MΩ



**Finding output impedance (Zo)**: . This expression tell us, first Vi input voltage must be set to zero volt (i.e. it should be connected to ground.) therefore, the circuit can further be drawn as follows to find Zo. Notice that since Vi is grounded (i.e. Vi->0 V), Vgs is also become 0 V. Therefore the current source of has become zero amper source which means that it can be assumed as “**open**” (see the figüre below).







Therefore Zo=RD||rd RD=1.8 k (since we assume rd->) is seen immediately from the circuit above.

b) Transconductance is given by



where from the Q3, we had IDSS=6 mA, VGSQ=-0.8 V, Vp=-3 V. Therefore, we have



c) From the ac eqvn. circuit we write

From which we calculate

d)

